

IN THE CLAIMS:

1. (currently amended) A semiconductor device, comprising:
 - a support substrate;
 - an insulating layer formed on the support substrate;
 - a first semiconductor layer formed on the insulating layer;
 - a first high breakdown voltage transistor formed in the first semiconductor layer,
the first high breakdown voltage transistor having a source and a drain;
 - a second semiconductor layer formed on the insulating layer;
 - a second high breakdown voltage transistor formed in the second semiconductor layer,
the second high breakdown voltage transistor having a source and a drain;
 - a first isolation region formed ~~through~~ between the first semiconductor layer and the second semiconductor layer, the first isolation region: being between the first and second high breakdown voltage transistors; contacting the source and the drain of each high breakdown voltage transistor; completely surrounding each of the first and second high breakdown voltage transistors individually; and having a depth that reaches the insulating layer;
 - a third semiconductor layer formed on the insulating layer;
 - a first low breakdown voltage transistor formed in the third semiconductor layer;
 - a second low breakdown voltage transistor formed in the third semiconductor layer; and
 - a second isolation region formed in the third semiconductor layer between the first low breakdown voltage transistor and the second first low breakdown voltage transistor, the second isolation region having a depth that does not reach the insulating layer.

2. (original) A semiconductor device according to Claim 1, further comprising:
a third isolation region formed between the second semiconductor layer and the third semiconductor layer, the third isolation region having a depth that reaches the insulating layer.
3. (original) A semiconductor device according to Claim 1,
wherein the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are all of equal thickness.
4. (original) A semiconductor device according to Claim 2,
wherein the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are all of equal thickness.
5. (original) A semiconductor device according to Claim 3,
wherein the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are respectively 500 to 2,000nm thick.
6. (original) A semiconductor device according to Claim 4,
wherein the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are respectively 500 to 2,000nm thick.
7. (original) A semiconductor device according to Claim 1,
wherein surfaces of the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are at a same level.

8. (original) A semiconductor device according to Claim 2,
wherein surfaces of the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are at a same level.
9. (original) A semiconductor device according to Claim 1,
wherein the first and second high breakdown voltage transistors further comprise:
a first gate insulating layer formed above a channel region; and
a second gate insulating layer formed above an offset region,
wherein the second gate insulating layer is thicker than the first gate insulating layer.
10. (original) A semiconductor device according to Claim 2,
wherein the first and second high breakdown voltage transistors further comprise:
a first gate insulating layer formed above a channel region; and
a second gate insulating layer formed above an offset region,
wherein the second gate insulating layer is thicker than the first gate insulating layer.
- Claims 11-19 (canceled).

20. (currently amended) A semiconductor device comprising:

a support substrate having a high breakdown voltage transistor region with a first isolation region and a second isolation region, wherein the first and second isolation regions are sized and configured to include one transistor per region;

an insulating layer formed on the support substrate;

a first high breakdown voltage transistor in the first isolation region;

a second high breakdown voltage transistor in the second isolation region; and

a low breakdown voltage transistor, wherein the first and second high breakdown voltage transistors are is within a first isolation region completely surrounded by the respective isolation region, wherein the first and second isolation regions have having a depth that reaches the insulating layer such that the first and second isolation regions isolates the first and second high breakdown voltage transistors from other transistors, and the low breakdown voltage transistor is adjacent to a second shallow isolation region having a depth that does not reach the insulating layer.

21. (withdrawn) A method of manufacturing a semiconductor device, the method comprising the steps of:

preparing a substrate including a support substrate and an insulating layer;

forming a first isolation region having a depth that reaches the insulating layer, wherein the first isolation region includes a first trench insulating layer;

forming a second isolation region having a depth that does not reach the insulating layer, wherein the second isolation region includes a second trench insulating layer;

forming a first high breakdown voltage transistor in a region within the first isolation region, wherein the first high breakdown voltage transistor includes a trench insulating offset; and

forming a first low breakdown voltage transistor in a region adjacent to the second isolation region,

wherein the first trench insulating layer, the second trench insulating layer and the trench insulating offset are all formed simultaneously.

Claims 22-25 (cancelled)

26. (currently amended) A semiconductor device according to Claim 1,

wherein the first semiconductor layer defines at least one trench that has a base part reaching the insulating layer and sidewalls extending through the insulating layer first semiconductor layer; and

further comprising a trench oxide film on the sidewalls of the at least one trench layer, wherein the trench oxide film has a lower end adjacent the insulating layer and an upper end that is rounded to favorably bury the at least one trench.